FORM-PTO-1390
(Rev. 10-96)

U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER: 032326-073

U.S. APPLICATION NO. (If known, see 37 C.F.R. 1.5): 09/601111 Unassigned

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/FR99/00054	14 January 1999	27 January 1998

TITLE OF INVENTION
MICROPROCESSOR CARD INCLUDING A CABLE COMMUNICATION CIRCUIT

APPLICANT(S) FOR DO/EO/US
Pascal COOREMAN, Stéphane RAYON and Bertrand GOMEZ

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This is an express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and the PCT Articles 22 and 39(1).
4. ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
5. ☒ A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. ☐ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☒ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US)
6. ☒ A translation of the International Application into English (35 U.S.C. 371(c)(2)).
7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☒ have not been made and will not be made.
8. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. ☒ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11. to 16. below concern other document(s) or information included:

11. ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. ☒ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. ☒ A FIRST preliminary amendment.
    ☐ A SECOND or SUBSEQUENT preliminary amendment.
14. ☐ A substitute specification.
15. ☐ A change of power of attorney and/or address letter.
16. ☐ Other items or information:

528 Rec'd PCT/PTO 27 JUL 2000

U.S. APPLICATION NO. (If known, see 37 C.F.R. 1.5)	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
Unassigned 09/601111	PCT/FR99/00054	032326-073

17. ☒ The following fees are submitted:	CALCULATIONS	PTO USE ONLY
Basic National Fee (37 CFR 1.492(a)(1)-(5)):		
Search Report has been prepared by the EPO or JPO $840.00 (970)		
International preliminary examination fee paid to USPTO (37 CFR 1.482) $670.00 (956)		
No international preliminary examination fee paid to USPTO (37 CFR 1.482) but international search fee paid to USPTO (37 CFR 1.445(a)(2)) $690.00 (958)		
Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO $970.00 (960)		
International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(2)-(4) $96.00 (962)		
ENTER APPROPRIATE BASIC FEE AMOUNT =	$ 840.00	
Surcharge of **$130.00 (154)** for furnishing the oath or declaration later than 20 ☐ 30 ☐ months from the earliest claimed priority date (37 CFR 1.492(e)).	$ -0-	

Claims	Number Filed	Number Extra	Rate		
Total Claims	5 -20 =	-0-	X$18.00 (966)	$ -0-	
Independent Claims	1 -3 =	-0-	X$78.00 (964)	$ -0-	
Multiple dependent claim(s) (if applicable)			+ $260.00 (968)	$ -0-	
TOTAL OF ABOVE CALCULATIONS =				$ 840.00	
Reduction for 1/2 for filing by small entity, if applicable. Verified Small Entity statement must also be filed. (Note 37 CFR 1.9, 1.27, 1.28).				$ -0-	
SUBTOTAL =				$ 840.00	
Processing fee of **$130.00 (156)** for furnishing the English translation later than 20 ☐ 30 ☐ months from the earliest claimed priority date (37 CFR 1.492(f)). +				$ -0-	
TOTAL NATIONAL FEE =				$ 840.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). **$40.00 (581)** per property +				$ 40.00	
TOTAL FEES ENCLOSED =				$ 880.00	
				Amount to be: refunded	$
				charged	$

a. ☒ A check in the amount of $ 880.00 to cover the above fees is enclosed.

b. ☐ Please charge my Deposit Account No. 02-4800 in the amount of $_____ to cover the above fees. A duplicate copy of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 02-4800. A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

James A. LaBarre
BURNS, DOANE, SWECKER & MATHIS, L.L.P.
P.O. Box 1404
Alexandria, Virginia 22313-1404

SIGNATURE

James A. LaBarre
NAME

28,632
REGISTRATION NUMBER

(09/99)

Patent
Attorney's Docket No. 032326-073

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	)	
	)	
Pascal COOREMAN et al	)	Group Art Unit: Unassigned
	)	
Application No.: Unassigned	)	Examiner: Unassigned
	)	
Filed: July 27, 2000	)	
	)	
For: MICROPROCESSOR CARD INCLUDING A CABLE COMMUNICATION CIRCUIT	)	

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Prior to examination and the calculation of filing fees, kindly amend the above-identified application as follows:

IN THE SPECIFICATION:

Page 1, immediately following the title, insert the following:

--This disclosure is based upon, and claims priority from French Patent Application No. 98/00858, filed January 27, 1998, and International Application No. PCT/FR99/00054, filed January 14, 1999, the contents of which are incorporated herein by reference.

Background of the Invention--.

Page 2, line 6, change "20" to --12--;

between lines 16 and 17, insert the heading:

--**Summary of the Invention** --.

Page 4, before line 1, insert the heading:

--**Brief Description of the Drawing**--;

between lines 7 and 8, insert the heading:

--**Detailed Description**--.

Page 10, delete numbered lines 21-23.

IN THE CLAIMS:

1. (Amended) A card [(30)] with a microprocessor [(10)] and contacts [(22)], [the microprocessor (10) communicating with a terminal (20) by means of] and a communication device [(40)] in the form of a hard-wired circuit disposed between the contacts [(22)] and the microprocessor [(10)] and operating according to an asynchronous communication protocol with checking of the integrity of [the] signals transmitted between the microprocessor and a terminal, [characterised in that] wherein said communication device [(40) comprises] includes means to return at least one item of information to the terminal [(20)] as a function of the signals received.

2. (Amended) A card with a microprocessor and contacts according to Claim 1, [characterised in that] wherein the communication device [(40)] comprises:

- a circuit [(34)] for analysing the electrical signals transmitted by [the] a terminal [(20)] so as to supply a series of electrical pulses,

- a circuit [(36)] for checking the series of electrical pulses in order to determine the integrity of the series of electrical pulses and to supply a code [(50)] indicating the status of the check,

- a circuit [(38)] for determining each character from the pulses in the series,

- a first plurality of registers [(42)] for recording the characters of [the] a command and [the] an address supplied by the character determination circuit [(38)] and making them available to the microprocessor [(10)],

- a second plurality of registers [(44)] for recording the characters of [the] data supplied by the character determination circuit [(38)] and making them available to the microprocessor [(10)],

- a circuit for acknowledging the command [(52)], associated with the first plurality of registers [(42)], for analysing the characters of the command and supplying a code [(54)] indicating [the] a command reception status,

- a third plurality of registers [(46)] for recording [the] codes for the data and for the status of execution of the command supplied by the microprocessor [(10)], and

- a circuit [(48)] for transmitting to the terminal [(20)] the codes supplied by the checking circuit [(36)], the command acknowledgement circuit [(52)] and the third plurality of registers [(46)].

3. (Amended) A card with microprocessor and contacts according to Claim 2, [characterised in that] wherein the analysis circuit [(34) comprises means to detect] detects the signals transmitted and [to present] presents them in the form of a series of electrical pulses of the binary type.

4. (Amended) A card with a microprocessor and contacts according to Claim 2 [or 3, characterised in that] wherein the checking circuit [(36) comprises means to check] checks for the presence [or not] of a binary parity digit or a cyclic redundancy code and [to supply] supplies a corresponding signal or code.

Add the following new claim:

--5. A card with a microprocessor and contacts card according to Claim 3, wherein the checking circuit checks for the presence of a binary parity digit or a cyclic redundancy code and supplies a corresponding signal or code.--

REMARKS

Entry of the foregoing amendments is respectfully requested. These amendments are intended to further clarify the language of the claims and specification. It is to be noted that the amendments have been made with respect to the claims as they appear in the annex to the International Preliminary Examination Report.

Respectfully submitted,

BURNS, DOANE, SWECKER & MATHIS, L.L.P.

By: _____
James A. LaBarre
Registration No. 28,632

P.O. Box 1404
Alexandria, Virginia 22313-1404
(703) 836-6620

Date: July 27, 2000

09/601111
528 Rec'd PCT/PTO 27 JUL 2000

V/PRTS

MICROPROCESSOR CARD INCLUDING A CABLE COMMUNICATION CIRCUIT

The invention relates to microprocessor cards which are capable of performing operations on data supplied by memories associated with the microprocessor or by a terminal to which they are connected.

In a simplified manner, a microprocessor 10 (see single figure) comprises a central unit 12 which communicates with a program memory 16, a data memory 18 and a memory 14 of the RAM type, RAM being the English acronym for "Random Access Memory". This microprocessor 10 is connected to a terminal 20 by means of a link 32 and a contact pin 22.

The electrical signals applied by the terminal 20 to the contact pin 22 are analysed by the microprocessor 10 by means of a special so-called communication program recorded in the program memory 16, this communication program being adapted to the

communication protocol which controls the exchanges of information between the card and the terminal in both directions.

Analysis of the electrical signals applied to the contact pin 22 constitutes a relatively lengthy task for the central unit 20, a task which mobilises a large part of the memories.

In a similar manner, the output of the information from the microprocessor 10 to the terminal 20 by means of the contact pin 22 also takes up the time of the central unit and space in the memories.

The aim of the present invention is therefore to produce a microprocessor card which does not have the aforementioned drawbacks so as to release time for the microprocessor for other tasks and to release memory capacity for these other tasks.

The invention lies in the fact that the communications between the terminal and the microprocessor card take place by means of a communication device, the said device being in the form of a hard-wired circuit.

The invention has the advantage of facilitating the development of a card and in particular reducing the qualification period and costs for it, the communication device, in the form of an independent part, being able to be qualified once and for all.

The invention relates to a microprocessor card with contacts, characterised in that the microprocessor communicates with the terminal by means of an

asynchronous communication device, the said communication device comprising:

- a circuit for analysing the electrical signals transmitted by the terminal so as to supply a series of electrical pulses,

- a circuit for checking the series of electrical pulses in order to determine the integrity of the series of electrical pulses and to supply a code indicating the status of the check,

- a circuit for determining each character from the pulses in the series,

- a first plurality of registers for recording the characters of the command and the address supplied by the character determination circuit and making them available to the microprocessor,

- a second plurality of registers for recording the characters of the data supplied by the character determination circuit and making them available to the microprocessor,

- a circuit for acknowledging the command, associated with the first plurality of registers, for analysing the characters of the command and supplying a code indicating the command reception status,

- a third plurality of registers for recording the codes for the data and for the status of execution of the command supplied by the microprocessor, and

- a circuit for transmitting to the terminal the codes supplied by the checking circuit, the command acknowledgement circuit and the third plurality of registers.

The invention will be understood more clearly by means of the following description of a particular example embodiment, the said description being given in relation to the accompanying drawing in which the single figure is a functional diagram of a microprocessor card having characteristics of the invention.

As indicated in the introduction, a microprocessor card 30 of the prior art comprises essentially a microprocessor 10 connected to a terminal 20 by means of a bidirectional link 32, depicted in dotted lines, and a contact connector 22. The binary electrical signals applied by the terminal 20 to the contacts 22 are analysed directly by the microprocessor 10. In addition, the binary electrical signals supplied by the microprocessor 10 are transmitted to the terminal 20 by means of the connection 32 and contacts 22.

In such an architecture, the microprocessor 10 acts directly in the bidirectional communication process, which presents certain drawbacks, notably those disclosed in the introduction.

According to the invention, the bidirectional communication process is implemented by a communication device 40, disposed between the contact terminals 22 and the microprocessor 10.

The communication device 40 comprises:

- a circuit 34 for analysing the electrical signals applied by the terminal 20 to the contact terminal 22 of the card 30; this circuit 34 analyses

the electrical signals appearing on the contacts 22 so as to present them in the form of a series of electrical pulses of the binary type;

- a circuit 36 for checking the series of binary electrical pulses in order to determine the integrity of the series of electrical pulses, that is to say to check whether the series is complete in accordance with predetermined rules, for example by the use of a binary parity digit or a redundant code in the series; this checking circuit 36 supplies a binary signal or a binary code indicating the result of this check on a link 50;

- a circuit 38 for determining each character of the command or instruction, address or data item from the pulses in the series checked;

- a first plurality of registers 42 for recording on the one hand the characters of the command or instruction and on the other hand the characters of the address, as they are determined by the determination circuit 38;

- a second plurality of registers 44 for recording the characters of the data supplied by the determination circuit 38;

- a circuit 52 for acknowledging the command associated with the first plurality of registers 42 in order to analyse the characters of the command or instruction and to supply a signal or binary code indicating the terminal or the faulty reception of the command on a link 54,

- a third plurality of registers 46 for recording on the one hand the data supplied by the microprocessor 10 and on the other hand the status code indicating the statuses of execution of the command by the microprocessor 10, and

- a circuit 48 for transmitting, to the terminal 10 by means of the contacts 22, the signals and/or codes supplied by the checking circuit 36 on the link 50, by the acknowledgement circuit 52 on a link 54 and by the third plurality of registers 46 on a link 56.

The different circuits making up the communication device 40 are adapted to the communication protocol chosen. This communication protocol is of the asynchronous type and can be the one known by the name of RS232, with regard to a serial link habitually used between a so-called personal computer and its peripherals, or by the names V22, V23, etc with regard to connection by modem.

In order to check the integrity of the series of pulses, the terminal 20 must be designed to add redundant information to the signals transmitted, information whose presence the checking circuit 36 is capable of checking. It may be a case of the presence of a parity bit or binary digit or a redundant cyclic code. It should be noted that many communication protocols make provision for such a redundancy in order to check the integrity of the information transmitted. Where this check is not successful, the command is not executed and this decision is indicated by a code on the link 50.

This integrity check relates only to the succession of binary digits corresponding to the pulses in the series; the check on the command is carried out by the acknowledgement circuit 52 which determines that the command is complete and correct and indicates this on the link 54 by a particular code. In the event of an error, the circuit 52 can indicate this by another particular code. These particular codes are transmitted to the transmission circuit 48 but also to the character determination circuit 38 in order to indicate to it, in the event of correct acknowledgement, that the following characters are to be switched to the second plurality of registers 44 provided for recording the data transmitted by the terminal after the command if the latter has indeed been received in its entirety.

[Translation of the Annex to the International Preliminary Examination Report]

CLAIMS

1. A card (30) with a microprocessor (10) and contacts (22), the microprocessor (10) communicating with a terminal (20) by means of a communication device (40) in the form of a hard-wired circuit disposed between the contacts (22) and the microprocessor (10) and operating according to an asynchronous communication protocol with checking of the integrity of the signals transmitted, characterised in that said communication device (40) comprises means to return at least one information to the terminal (20) as a function of the signals received.

2. A card with a microprocessor and contacts according to Claim 1, characterised in that the communication device (40) comprises:

- a circuit (34) for analysing the electrical signals transmitted by the terminal (20) so as to supply a series of electrical pulses,
- a circuit (36) for checking the series of electrical pulses in order to determine the integrity of the series of electrical pulses and to supply a code (50) indicating the result of the check,
- a circuit (38) for determining each character from the pulses in the series,
- a first plurality of registers (42) for recording the characters of the command and the address supplied by the character determination

circuit (38) and making them available to the microprocessor (10),

- a second plurality of registers (44) for recording the characters of the data supplied by the character determination circuit (38) and making them available to the microprocessor (10),

- a circuit for acknowledging the command (52), associated with the first plurality of registers (42), for analysing the characters of the command and supplying a code (54) indicating the command reception status,

- a third plurality of registers (46) for recording the codes for the data and for the status of execution of the command supplied by the microprocessor (10), and

- a circuit (48) for transmitting to the terminal (20) the codes supplied by the checking circuit (36), the command acknowledgement circuit (52) and the third plurality of registers (46).

3. A card with a microprocessor and contacts according to Claim 2, characterised in that the analysis circuit (34) comprises means to detect the signals transmitted and to present them in the form of a series of electrical pulses of the binary type.

4. A card with a microprocessor and contacts according to Claim 2 or 3, characterised in that the checking circuit (36) comprises means to check the presence or not of a binary parity digit or a cyclic redundancy code and to supply a corresponding signal or code.

ABSTRACT

A MICROPROCESSOR CARD INCLUDING A HARD-WIRED COMMUNICATION CIRCUIT

The invention relates to cards with a microprocessor (10) and contacts (22).

The invention lies in the fact that a communication device (40) of the asynchronous type is disposed between the contacts (22) and the microprocessor (10) so as to relieve the microprocessor of the communication tasks and thus allow better use of the central unit (12) of the microprocessor (10) and the associated memories (14, 16, 18). This device (40) comprises essentially an analysis circuit (34), a circuit (36) for checking the integrity of the series of pulses, a circuit (38) for determining the characters in the series of pulses and pluralities of registers (42, 44 and 46) which are connected with the microprocessor (10).

The invention is applicable to microprocessor smart cards.

Single figure.

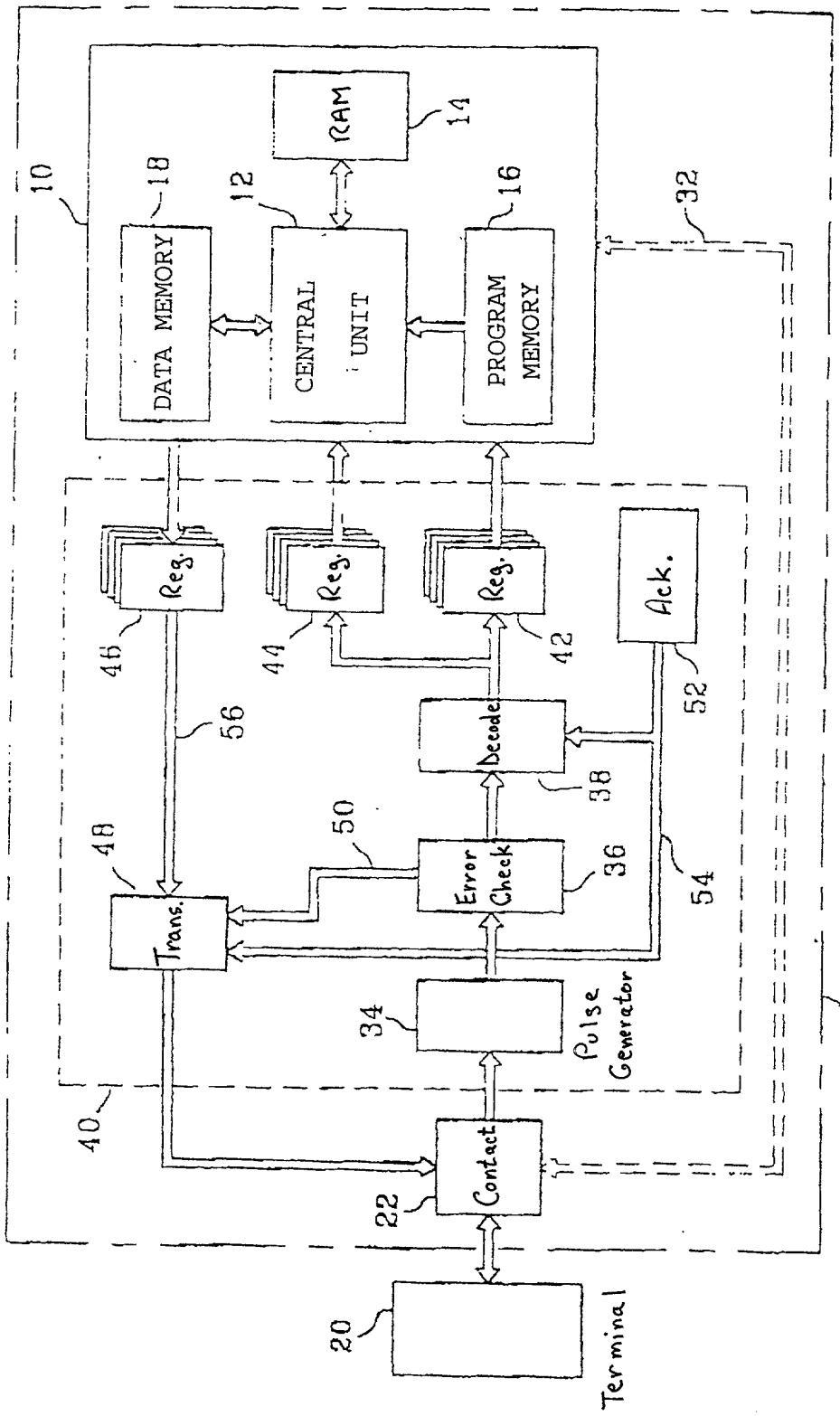
10
RAM
14
18
12
16
32
DATA MEMORY
CENTRAL UNIT
PROGRAM MEMORY
Reg.
Reg.
Reg.
Ack.
46
44
42
52
56
decode
38
48
50
Error Check
36
54
Trans.
34
Pulse Generator
30
40
Contact
22
20
Terminal

FIG. 1

greee 11

COMBINED DECLARATION FOR PATENT APPLICATION AND POWER OF ATTORNEY (Includes Reference to Provisional and PCT International Applications)	Attorney's Docket No.

As a below named inventor, I hereby declare that:
My residence, post office address and citizenship are as stated below next to my name;
I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

MICROPROCESSOR CARD INCLUDING A CABLE COMMUNICATION CIRCUIT

the specification of which (check only one item below):

- is attached hereto.
- was filed as United States application
  Number _____
  on _____
  and was amended
  on _____ (if applicable).
- was filed as PCT International application
  Number PCT/FR99/00854
  on 31.01.99.
  and was amended
  on _____ (if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, §1 56.

I hereby claim foreign priority benefits under Title 35, United States Code, §119 (a)-(e) of any foreign application(s) for patent or inventor's certificate or of any PCT international application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed:

PRIOR FOREIGN/PCT APPLICATION(S) AND ANY PRIORITY CLAIMS UNDER 35 U.S.C. §119:

COUNTRY (if PCT, indicate "PCT")	APPLICATION NUMBER	DATE OF FILING (day, month, year)	PRIORITY CLAIMED UNDER 35 U.S.C. §119
PCT	WO 99/38116	29.07.99.	_Yes _No
FRANCE	98 00858	27.01.1998	_Yes _No
			_Yes _No
			_Yes _No
			_Yes _No

I hereby claim the benefit under Title 35, United States Code §119 (e) of any United States provisional application(s) listed below.

_____ _____
(Application Number) (Filing Date)

_____ _____
(Application Number) (Filing Date)

(1/00)

COMBINED DECLARATION FOR PATENT APPLICATION AND POWER OF ATTORNEY (CONT'D) (Includes Reference to Provisional and PCT International Applications)	Attorney's Docket No.

I hereby claim the benefit under Title 35, United States Code, §120 of any United States applications(s) or PCT International application(s) designating the United States of America that is/are listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in that/those prior application(s) in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose to the Office all information known to me to be material to the patentability as defined in Title 37, Code of Federal Regulations §1.56, which became available between the filing date of the prior application(s) and the national or PCT International filing date of this application:

PRIOR U.S. APPLICATIONS OR PCT INTERNATIONAL APPLICATIONS DESIGNATING THE U.S. FOR BENEFIT UNDER 35 U.S.C. §120:

U.S. APPLICATIONS		STATUS (check one)		
U.S. APPLICATION NUMBER	U.S. FILING DATE	PATENTED	PENDING	ABANDONED
PCT APPLICATIONS DESIGNATING THE U.S.				
PCT APPLICATION NO.	PCT FILING DATE	U.S. APPLICATION NUMBERS ASSIGNED (if any)		
WO 99/38116	29.07.99			

I hereby appoint the following attorneys and agent(s) to prosecute said application and to transact all business in the Patent and Trademark Office connected therewith and to file, prosecute and to transact all business in connection with international applications directed to said invention:

William L. Mathis	17,337	R. Danny Huntington	27,903	Gerald F. Swiss	30,113
Robert S. Swecker	19,885	Eric H. Weisblatt	30,505	Michael J. Ure	33,089
Platon N. Mandros	22,124	James W. Peterson	26,057	Charles F. Wieland III	33,096
Benton S. Duffett, Jr.	22,030	Teresa Stanek Rea	30,427	Bruce T. Wieder	33,815
Norman H. Stepno	22,716	Robert E. Krebs	25,885	Todd R. Walters	34,040
Ronald L. Grudziecki	24,970	William C. Rowland	30,888	Renni S. Jillions	31,979
Frederick G. Michaud, Jr.	26,003	T. Gene Dillahunty	25,423	Harold R Brown III	36,341
Alan E. Kopecki	25,813	Patrick C. Keane	32,858	Allen R. Baum	36,086
Regis E. Slutter	26,999	Bruce J. Boggs, Jr.	32,344	Steven M. duBois	35,023
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Robert G. Mukai	28,531	Peter K Skiff	31,917	Kenneth B. Leffler	36,075
George A. Hovanec, Jr.	28,223	Richard J. McGrath	29,195	Fred W. Hathaway	32,236
James A. LaBarre	28,632	Matthew L. Schneider	32,814		
E. Joseph Gess	28,510	Michael G. Savage	32,596		

21839

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Address all telephone calls to: James A. LaBarre at (703) 836-6620.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

COMBINED DECLARATION FOR PATENT APPLICATION AND POWER OF ATTORNEY (CONT'D) (Includes Reference to Provisional and PCT International Applications)	Attorney's Docket No.

FULL NAME OF SOLE OR FIRST INVENTOR PASCAL SOONEMAN	SIGNATURE	DATE 29/6/00
RESIDENCE Les Jardins de l'Enfant.	CITIZENSHIP FRANCE.	
POST OFFICE ADDRESS Les Jardins de l'Enfant 23, av Beau Rivage 13008 Marseille.		
FULL NAME OF SECOND JOINT INVENTOR, IF ANY STEPHANE RAYON	SIGNATURE	DATE 04/07/00
RESIDENCE Les Hauts de Frioul les chemin de la Garde	CITIZENSHIP FRANCE	
POST OFFICE ADDRESS les Hauts de Frioul chemin de la Garde 13600 La Ciotat.		
FULL NAME OF THIRD JOINT INVENTOR, IF ANY BERTRAND GOMEZ	SIGNATURE	DATE 04-7-00
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POST OFFICE ADDRESS 713, chemin des Baraques. 13360 ROQUEVAIRE		
FULL NAME OF FOURTH JOINT INVENTOR, IF ANY	SIGNATURE	DATE
RESIDENCE	CITIZENSHIP	
POST OFFICE ADDRESS		
FULL NAME OF FIFTH JOINT INVENTOR, IF ANY	SIGNATURE	DATE
RESIDENCE	CITIZENSHIP	
POST OFFICE ADDRESS		
FULL NAME OF SIXTH JOINT INVENTOR, IF ANY	SIGNATURE	DATE
RESIDENCE	CITIZENSHIP	
POST OFFICE ADDRESS		
FULL NAME OF SEVENTH JOINT INVENTOR, IF ANY	SIGNATURE	DATE
RESIDENCE	CITIZENSHIP	
POST OFFICE ADDRESS		
FULL NAME OF EIGHTH JOINT INVENTOR, IF ANY	SIGNATURE	DATE
RESIDENCE	CITIZENSHIP	
POST OFFICE ADDRESS		